a) General Technology: Sacrificial layer Contact (CMOS-) Substrate (CMOS-) Substrate ALD layer(s) Sacrificial layer Contact (CMOS-) Substrate

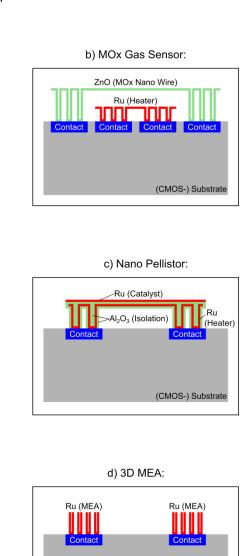


Fig. 1: Cross section (not on scale) of the technology and the three applications.

(CMOS-) Substrate

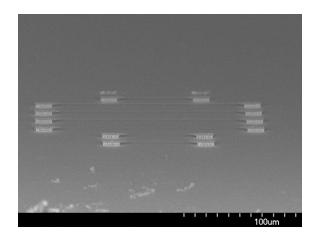
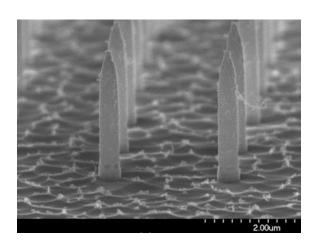


Fig. 2: SEM-image of a 350 nm wide and 150 μm long Ru nano wire.



(CMOS-) Substrate

Fig. 3: SEM-image of 3D MEA with a tip diameter of 100 nm.