ALD Applications
Room On Demand - Session AA4
Applications in ULSI FEOL: High-k

AA4-1 Plasma Impact on the HfO_2 High-K Dielectric: Continuous-Wave Plasma Etch Versus Quasi-Atomic Layer Etch, ***Dunja Radisic***, *Q. Smets, T. Schram,* IMEC, Belgium

Etch stop layers (ESL) are commonly used to protect critical films. This is also the case for 300 mm 2D material integration where HfO_2 ESL is used first for the contact trench etch, and again for the damascene high-k first/top gate last process steps. For the latter, the HfO_2 ESL also serves as top gate dielectric and is hence highly sensitive to plasma-induced damage (PID).

In this paper, two main approaches were investigated for the SiO_2 removal stopping on HfO_2. Conventional, Continuous-Wave (CW) plasma experiments (Fluorine-based) were performed in the ICP, and the Quasi-Atomic Layer Etch (Q-ALE) in CCP reactor, both from Lam Research Corporation. The goal was to explore Q-ALE and make a general comparison between the two approaches. The advantage of ALE, as well as Q-ALE over CW plasma etch is its unique capability to remove the material with an angstrom precision, causing minimal or no damage and material removal with high etch selectivity.

Simple metal oxide metal capacitor (MIMCAP) test vehicle was used for the study. First, a 10nm TiN bottom electrode was deposited on Silicon wafers, followed by a 10nm HfO_2 layer and a SiO_2 hard mask. The SiO_2 is etched with a spin-on carbon/spin-on glass/photoresist stack, stopping on the underlying HfO_2. Following the plasma processing, the TiN/W top electrode metal stack is deposited in the trenches, and planarized with chemical mechanical polishing (CMP) to electrically isolate the devices.

Our results show that for the CW approach, longer over-etch (OE) thins the HfO_2, and consequently, increases the leakage current and lowers the breakdown voltage. In the case of Q-ALE, the HfO_2 thickness is intact even with the prolonged OE, implying high process selectivity to HfO_2, with no morphological or electrical evidence of PID. However, in the case of Q-ALE, longer OE causes more spread in the electrical performance. This is likely the result of more residues, formed during the passivation step, and remaining on the HfO_2 surface after processing. (Further process performance improvement can be potentially achieved using the effective post-plasma cleaning, but it was not the goal of this study).

We conclude that Q-ALE is a promising technique for the applications where the HfO_2 ESL also serves as the gate oxide. The high etch selectivity and low PID make it ideal for novel integration flows, like 300 mm 2D material integration.

AA4-2 Self-Aligned Atomic Layer Deposited Gate Stacks for Electronic Applications, ***Amy Brummer***, *A. Mohabir, M. Filler, E. Vogel,* Georgia Institute of Technology

The formation of self-aligned MOSFET gate stacks via area-selective atomic layer deposition (AS-ALD) of high-κ dielectric and metal films offers a route to reduce the number of lithography steps, maintain a low thermal budget, and improve performance by eliminating overlap capacitance. In this work, a new method for bottom-up masking of semiconductor surfaces and nano/microstructures is combined with AS-ALD to fabricate a high-performance gate stack that is self-aligned to the underlying doped source-drain regions. We begin with the SCALES process, which involves a poly(methyl methacrylate) (PMMA) brush grown from a silicon surface [1]. The PMMA brush is then patterned via a mild selective etching of the underlying semiconductor based on the Si dopant concentration. KOH etches lightly doped Si much faster than heavily doped Si, allowing for selective removal from only the lightly doped regions. The full gate stack is then deposited via AS-ALD in areas where the brush has been removed, as shown in Figure 1. Figure 2 shows XPS data of an example gate stack sequence deposited via AS-ALD, including a HfO_2 dielectric and a Pt gate electrode. Both spectra show good selectivity of deposition toward the regions where PMMA had been removed. Figure 3 shows the C-V characteristics of a gate stack on both a silicon substrate that did not undergo the PMMA process as well as a silicon substrate in which the PMMA was removed via etching. The C-V characteristics are almost identical for both cases indicating that the PMMA brush growth and removal does not strongly impact the silicon-HfO_2 interface. The maximum capacitance was used to determine a relative dielectric constant of ~24 which is expected for HfO_2. The interface state density was extracted from the C-V characteristics to be on the order of 10^{12} cm^{-2}. Ongoing work aims to reduce defect density in this and other high-κ dielectrics (e.g. TiO_2, Al_2O_3, ZrO_2).

[1] Mohabir, Amar T., et al. "Bottom-Up Masking of Si/Ge Surfaces and Nanowire Heterostructures via Surface-Initiated Polymerization and Selective Etching." ACS nano 14.1 (2020): 282-288.

AA4-3 Film Characteristics of Lanthanide Oxide Thin Film by Using Atomic Layer Deposition Method, ***Se-Won Lee***, *M. Kim,* Merck Electronics, Korea (Republic of); *S. Ivanov,* EMD Electronics

Lanthanide oxide films possess a wide variety of functional properties. In particular, using them as insulators in MIM structures offers a number of advantages over silicon dioxide. Lanthanide oxide based thin films can be used as gas sensors or hard mask. They are potentially attractive materials for the fabrication of multi layer optical coatings, beam splitters, passive components of integrated circuits, and heat based laser recording devices. Among them, terbium oxide (Tb_2O_3) and gadolinium oxide (Gd_2O_3) have proven to be promising materials for conventional silicon dioxide replacement in nano device applications. It has a relatively high dielectric constant (14 ~ 20) and a large band gap. Our research examines the electrical and physical characteristics of TbO_x and GdO_x thin film by atomic layer deposition (ALD) with as-dep and post rapid thermal annealing (RTP) to improve dielectric characteristics and optimize performance for potential application in nano devices.

Here, we report thermal ALD of TbO_x and GdO_x thin films using high purity Tris(i-propylcyclopentadienyl) terbium(III) (Tb(iPrCp)3) and Tris(i-propylcyclopentadienyl)gadolinium(III) (Gd(iPrCp)3). Deposition of both films was investigated by thermal ALD process with ozone reactant at 150-350 °C on Si and TiN substrates. After film deposition, RTP was conducted to observe post annealing effects. Some ALD conditions, including ALD window, and other film properties were very similar to the two films. In both films, amorphous phase with no XRD peak was observed at 200 °C samples, but crystallization peak was observed over 250 °C. The film density of GdO_x film was ~ 15% higher than the TbO_x film. XPS results showed that carbon is detected in 200 °C samples, but it is not detected at temperatures above that. Both samples showed a good step coverage of more than 90% at 200°C, but step coverage was deteriorated rapidly in samples of more than 250°C. Dielectric constant was measured by TiN/TbO_x or GdO_x/TiN (MIM) structure.

As a result, we conducted atomic layer deposition of lanthanide oxide, TbO_x and GdO_x films and analyzed its properties. Both films showed low process temperatures of 200 °C, good step coverage, and high dielectric constant, so these characteristics are expected to be used in applications such as high-k gate insulators or hard mask.

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