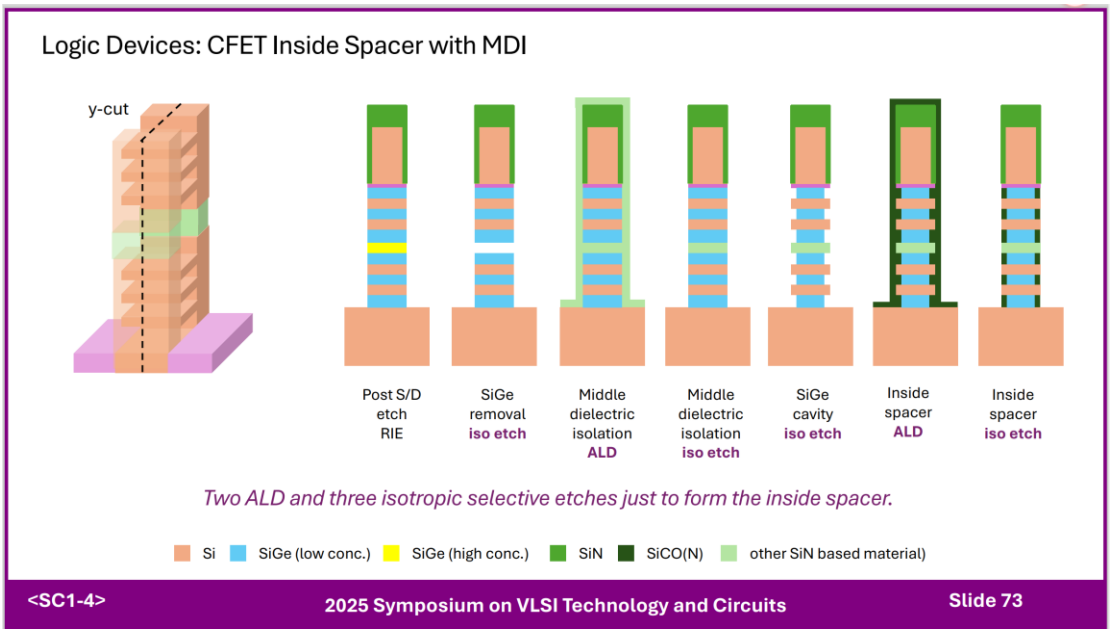

T.Lill, VLSI (2025).

Fig1 Publicly available MDI and Inner spacer process flow

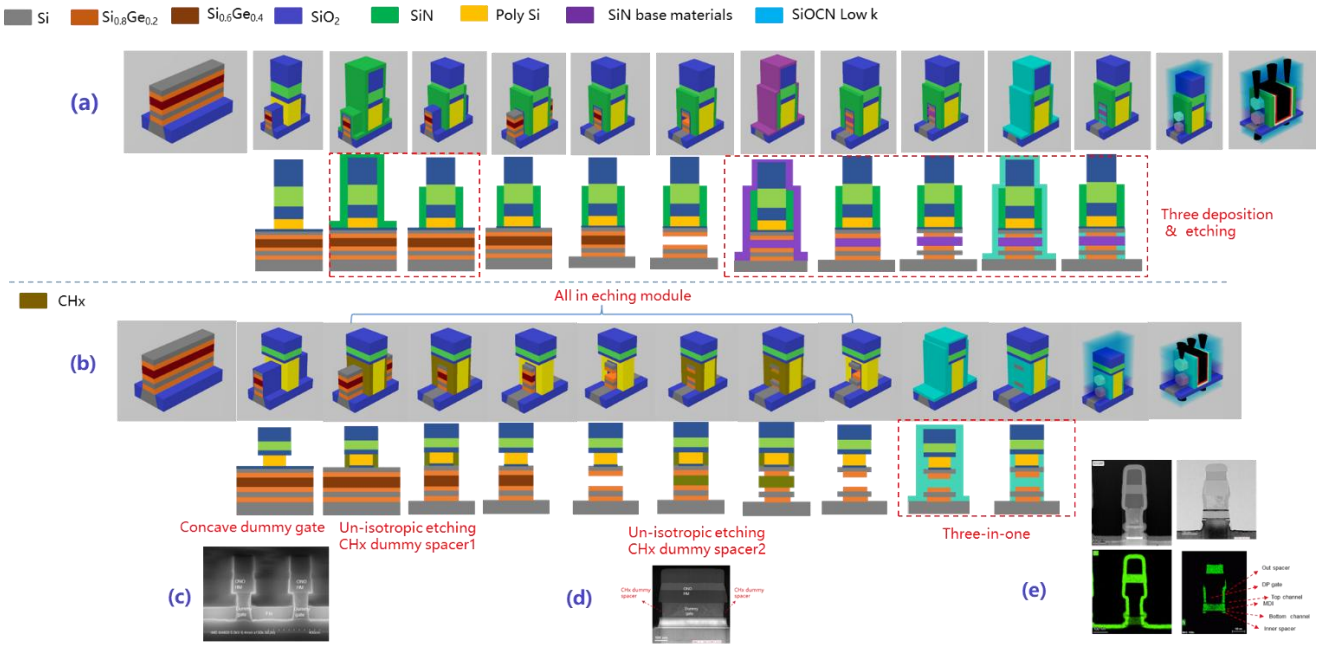

Figure 2 (a) shows the typical CFET process flow; (b) shows this article three-in-one new integration process flow; (c) shows the concave dummy gate; (d) shows CHx dummy spacer self-aligned etching S/D in the intermediate steps of the key process; (e) Three-in-one TEM of experimental structure