

AI/ML/Autonomous Experimentation for Thin Films Processing

Room 317 - Session AIML1-FrM

Materials Design and Autonomous Discovery

Moderator: Eden Goodwin, Carleton University, Canada

8:15am **AIML1-FrM-1 Accelerating Discovery and Design for Thin Film Polymer Self-Assembly through Machine Learning**, *Gregory Doerk*, Brookhaven National Laboratory **INVITED**

Thin film polymer self-assembly is a powerful approach to create nanoscale patterns across large areas with low cost for diverse applications in electronics and materials science. The confluence of compositional and architectural variation, entropic and surface energy constraints arising from thin film confinement, and process-dependent assembly pathways yields of panoply of nanoscale morphologies of which only a fraction can be discovered, catalogued, and engineered through manual experimentation. This talk will elaborate examples where artificial intelligence and machine learning (AI/ML) can accelerate thin film polymer self-assembly research. We describe the application of Gaussian process regression to automate x-ray scattering characterization for the discovery of new morphologies in template-directed self-assembly of block copolymer blends. We then illustrate the application of an active learning approach that incorporates foundation model-supported “few shot” image classification for determining processing-morphology relationships in spray-deposited block copolymer/homopolymer blend films using minimal quantities of data. Complementary in situ x-ray scattering measurements during spraying provide key mechanistic insights into trends in self-assembled structural organization across the process design space.

8:45am **AIML1-FrM-3 Spatially Resolved, Machine Learned Virtual Metrology Yielding Significant Process Control Benefit in Volume Wafer Processing**, *Michael Koltonski, Daniel Chalom, Thomas Li, Pratik Kotcher*, Applied Materials; *William Wang*, Applied Materials, Taiwan; *Crystal Huang*, Applied Materials

High volume semiconductor manufacturing is capital limited with respect to external metrology sampling. The industry has considerable interest developing and utilizing virtual metrology of wafer processing, significantly increasing sampling which provides opportunity for low latency-high sampling integrated process control. The challenge for developing this ecosystems for plasma dry etch wafer processing is that the critical wafer processes typical require spatial virtual metrology, and commercial plasma dry etch reactors are not designed to meet this need due to cost and/or technical complexity.

Our team developed an on-tool, spatially resolved sensor, when combined with machine learning modeling creates spatially resolved virtual metrology. Through method development, these virtual metrology models have sufficient accuracy that when combined with an integrated, on-demand, closed loop process controller, the resulting process capability of the wafer process in volume improved by >50%. This result demonstrated on an advanced DRAM node critical patterning application. Deploying this technology at critical wafer processing applications should accelerate yield ramp during pilot manufacturing and maximize good die outs during peak volume manufacturing.

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