

International Workshop on Gallium Oxide and Related Materials (IWGO-6)

Room ESJ 0202 - Session IWGO-WeA

Advanced Device Scaling and Fabrication Techniques I

Moderators: Siddharth Rajan, The Ohio State University, Yuhao Zhang, University of Hong Kong

2:00pm IWGO-WeA-1 Recent Advances in β -Ga₂O₃ Power and RF Device Technologies, Uttam Singiseti, University at Buffalo INVITED

The ultrawide-bandgap semiconductor β -gallium oxide (Ga_2O_3) has emerged as a promising material for power electronics, RF, and high-speed switching applications. This talk presents recent advances in Ga_2O_3 device technologies developed by our group. We demonstrate lateral Ga_2O_3 MOSFETs incorporating optimized field-plate designs that achieve beyond-kilovolt breakdown voltages, along with their switching characteristics under electrical stress conditions. The role of in situ Mg-doped MOCVD-grown Ga_2O_3 films as efficient current-blocking layers (CBLs) is discussed. In addition, trench MOSFET architectures incorporating CBLs are presented for high-voltage, high-speed operation targeting grid-level power applications. Strategies for mitigating thermal management challenges in Ga_2O_3 devices are also addressed.

Owing to its high Johnson's figure of merit, Ga_2O_3 is also a strong candidate for high power density RF amplifiers. We report significant improvements in RF power performance using Ga_2O_3 technology. By aggressively scaling gate lengths and gate-source spacing, $(\text{Al}_x\text{Ga}_{1-x})_2\text{O}_3/\text{Ga}_2\text{O}_3$ heterostructure FETs were fabricated, demonstrating record RF performance. We will also report the radiation tolerance of the RF devices.

2:25pm IWGO-WeA-6 1.5 kV/0.6 A Double Pulse Test Switching Of $\text{Cr}_2\text{O}_3/\beta\text{-Ga}_2\text{O}_3$ Heterojunction Diodes With > 3 kV Breakdown Voltages And Record Low Reverse Recovery Charge, Chinmoy Nath Saha, University of California Santa Barbara; Yuzhou Yao, Juchen Yang, The Ohio State University; Yizheng Liu, University of California at Santa Barbara; Pengyu Fu, Shuwei He, The Ohio State University; James S. Speck, University of California at Santa Barbara; Jin Wang, The Ohio State University; Sriram Krishnamoorthy, University of California at Santa Barbara

$\beta\text{-Ga}_2\text{O}_3$ heterojunction diodes (HJD) incorporating different p-type oxides (NiO_x , Cu_2O , Cr_2O_3) have been demonstrated with multi-kV-class breakdown voltages. In this work, we report the first experimental demonstration of kV-class static and switching performance of $\text{Cr}_2\text{O}_3/\beta\text{-Ga}_2\text{O}_3$ heterojunction diodes (HJD) with > 3 kV breakdown voltages. The devices were fabricated on (001)-oriented 9.5 μm thick $\beta\text{-Ga}_2\text{O}_3$ drift layer grown by halide vapor phase epitaxy (HVPE) on a conductive $\beta\text{-Ga}_2\text{O}_3$ substrate. Bi-layer Cr_2O_3 and anode metal ($\text{Ni}/\text{Au}/\text{Ni}$) were lifted off simultaneously to fabricate the HJD. A 1.5 μm mesa etch was employed to realize an effective edge termination. The fabricated HJDs exhibited a forward current density of 125 A/cm^2 at 4.5 V and a differential specific on-resistance of $\sim 19 \text{ m}\Omega\cdot\text{cm}^2$. Breakdown voltage of $\sim 3.2 \text{ kV}$ was achieved for a wide range of device dimensions (diameter = 60-300 μm) with noise floor reverse leakage up to 2.5-3 kV. This is a significant achievement since breakdown voltage showed no substantial degradation with increasing device dimensions [1]. Based on a punch-through model, the estimated parallel-plane breakdown field approached $\sim 4 \text{ MV}/\text{cm}$. In addition, the switching performance of $\beta\text{-Ga}_2\text{O}_3$ power diodes is critical for high-frequency power conversion applications. A double pulse test (DPT) was employed, where Ga_2O_3 HJD served as the upper device and a commercially available SiC MOSFET served as the lower switching device. At a reverse voltage of 1.5 kV and a peak forward current of about 0.6 A, the HJD showed a peak reverse recovery current (I_{rr}) of -0.128 A , a reverse recovery time (t_{rr}) of 12.8 ns, and an ultralow reverse recovery charge (Q_{rr}) of 0.74 nC. This is the highest test voltage and lowest reverse recovery charge reported for the $\beta\text{-Ga}_2\text{O}_3$ diode switching test. Additional measurements at 1 kV with peak forward currents ranging from 0.3 to 0.7 A showed relatively stable I_{rr} , t_{rr} , Q_{rr} at 0.1 A, 15 ns, and 0.6 nC, respectively. In comparison with a commercial SiC MPS diode exhibiting Q_{rr} of 41 nC and t_{rr} of 20 ns at 1.2 kV, the $\text{Cr}_2\text{O}_3/\beta\text{-Ga}_2\text{O}_3$ HJDs reported here show improved reverse recovery characteristics. In summary, we have achieved > 3 kV breakdown voltages with 4 MV/cm parallel plane electric field for a wide range of device dimensions by fabricating $\text{Cr}_2\text{O}_3/\beta\text{-Ga}_2\text{O}_3$ heterojunction diodes (HJD) with an optimized edge termination. The combination of multi-kV static breakdown voltages with sub-nC reverse recovery charge at 1.5 kV test voltage highlights the strong potential of $\text{Cr}_2\text{O}_3/\beta\text{-Ga}_2\text{O}_3$ HJDs for future medium-voltage and high-frequency power conversion applications.

[1]. Liu, AIP Advances, **15**, 015114 (2025).

2:40pm IWGO-WeA-9 Sub-Micron $\beta\text{-Ga}_2\text{O}_3$ FinFETs with >700 mA/mm Current Density and > 10^8 ON/OFF Ratio Using Si δ -Doped Channels, Nabasindhu Das, Arizona State University

$\beta\text{-Ga}_2\text{O}_3$ is a promising ultra-wide bandgap semiconductor for RF/mm-wave transistors due to its large critical breakdown field ($\sim 8 \text{ MV}/\text{cm}$), high saturation velocity ($\sim 2 \times 10^7 \text{ cm}/\text{s}$), and availability of bulk substrates. However, achieving high current density and strong electrostatic control in scaled devices remains challenging with uniformly doped channels due to short-channel effects. In this work, we demonstrate sub-micron gated depletion-mode $\beta\text{-Ga}_2\text{O}_3$ FinFETs employing Si δ -doped channels with sheet charge density exceeding $3 \times 10^{13} \text{ cm}^{-2}$, enabling enhanced carrier confinement and improved device performance. The δ -doped epitaxial structure was grown by MOCVD as shown in Fig.1 (b). Fin structures with 100 nm width and 200 nm spacing were defined using e-beam lithography and ICP-RIE etching (Fig.1 a, c). Ohmic contact regrowth was used to achieve low contact resistance, followed by ALD deposition of a 7 nm Al_2O_3 gate dielectric and fabrication of sub-micron gates ($L_g \approx 150 \text{ nm}$). Hall measurements indicate a sheet carrier density of $\sim 3.3 \times 10^{13} \text{ cm}^{-2}$ with mobility of $\sim 89 \text{ cm}^2/\text{V}\cdot\text{s}$. Devices exhibit low contact resistance and a sharp doping profile with $\sim 4.8 \text{ nm}$ FWHM. Transfer characteristics show clear pinch-off with threshold voltage $\sim -17 \text{ V}$, subthreshold slope $\sim 239 \text{ mV}/\text{dec}$, and ON/OFF ratio exceeding 10^8 with low gate leakage. Output characteristics demonstrate current saturation with peak drain current $>700 \text{ mA}/\text{mm}$. Pulsed I-V measurements reveal $\sim 20\%$ current collapse, indicating the need for improved surface passivation. Small-signal RF measurements yield $f_T \approx 6.3 \text{ GHz}$ and $f_{\text{MAX}} \approx 2 \text{ GHz}$. These results highlight the potential of δ -doped $\beta\text{-Ga}_2\text{O}_3$ FinFETs as promising platform for high power RF applications. This work is supported by the Army Research Office UWBG RF center under award No. W911NF2520005

2:55pm IWGO-WeA-12 Over 3 kV Ultra-low Leakage Vertical (011) $\beta\text{-Ga}_2\text{O}_3$ Diodes with Schottky Contact Engineering and High-k Field Plate, Emerson Hollar, Esmat Farzana, Iowa State University

The $\beta\text{-Ga}_2\text{O}_3$ has achieved great interest for high-power devices due to its large critical breakdown field, shallow dopants, and melt-grown native substrates. To achieve the desired multi-kV $\beta\text{-Ga}_2\text{O}_3$ power switches, vertical devices with low-doped, thick drift layer and minimal defects are essential requirements. However, to date, scaling up the voltage rating of vertical $\beta\text{-Ga}_2\text{O}_3$ devices has remained severely limited due to the presence of killer dislocation defects and unintentional [Cl] impurities that creates difficulties in achieving high-quality thick drift layer ($>10 \mu\text{m}$) and lower doping ($<8 \times 10^{15} \text{ cm}^{-3}$) with the existing (001) $\beta\text{-Ga}_2\text{O}_3$ epiwafers grown by halide vapor phase epitaxy (HVPE). To overcome these constraints, the recently emerged HVPE (011) $\beta\text{-Ga}_2\text{O}_3$ epiwafers has brought tremendous potential by offering reduced dislocation effects due to the dislocation being parallel to the (011) plane as well as low unintentional [Cl] impurities [1]. However, due to their early stage, high-power vertical Schottky barrier diodes (SBD) on (011) $\beta\text{-Ga}_2\text{O}_3$ epiwafers are yet to be reported.

In this work, we report high-voltage vertical (011) $\beta\text{-Ga}_2\text{O}_3$ SBDs on HVPE-grown 20 μm thick drift layer with 1 MHz C-V extracted doping $\sim 5 \times 10^{15} \text{ cm}^{-3}$. Two different Schottky contact diodes were co-fabricated with 100 μm diameters, including Pt/ $\beta\text{-Ga}_2\text{O}_3$ and $\text{PtO}_x/\text{thin Pt}$ (1.5 nm)/ $\beta\text{-Ga}_2\text{O}_3$. The $\text{PtO}_x/\text{thin Pt}$ contact merges the benefits of both low turn-on voltage from interfacing Pt while allowing improved reverse blocking by PtO_x [1]. To reduce edge field crowding, we integrated high-permittivity (κ) ZrO_2 field-plate (FP) for both contacts using a stack of sputtered ZrO_2 (226 nm) on interfacing thin ZrO_2 (9 nm) formed by atomic layer deposition to protect the surface from sputter damage. The forward J-V showed excellent transport properties with near unity ideality factor and similar turn-on voltage for both cases. At reverse bias, the SBDs without FP revealed similar breakdown voltage of $\sim 1.5 \text{ kV}$ for both cases. However, with FP, the $\text{PtO}_x/\text{thin Pt}$ SBDs showed significantly enhanced breakdown voltage $\sim 3.7 \text{ kV}$ compared to the Pt ones (2.75 kV) and punch-through field with a peak of 5 MV/cm at FP edge, reaching ZrO_2 breakdown limit. Moreover, the FP $\text{PtO}_x/\text{thin Pt}$ SBDs demonstrated ultra-low leakage which is order of magnitude lower compared to existing reports of (001) $\beta\text{-Ga}_2\text{O}_3$ SBDs of same 100 μm diameter at 3 kV operation. **To the best of our knowledge, this is the first report of high-power vertical (011) $\beta\text{-Ga}_2\text{O}_3$ SBDs that shows its great potential to expand the performance limit of low-loss multi-kV $\beta\text{-Ga}_2\text{O}_3$ devices.**

[1] E. J. Hollar and E. Farzana, *Appl. Phys. Lett.* **128**, 053503 (2026).

3:10pm IWGO-WeA-15 Vertical Ga₂O₃(010) FinFETs Processed with Nitrogen Radical Irradiation, **Zhenwei Wang**, National Institute of Information and Communications Technology, Japan; *Jin Inajima, Kohki Tsujimoto, Yusuke Teramura*, Osaka Metropolitan University, Japan; *Yoshiki Iba, Yuma Terauchi*, Tokyo University of Agriculture and Technology, Japan; *Junya Yoshinaga*, Tokyo University of Agriculture and Technology/TAIYO NIPPON SANSO CORPORATION, Japan; *Takafumi Kamimura*, National Institute of Information and Communications Technology, Japan; *Yoshinao Kumagai*, Tokyo University of Agriculture and Technology, Japan; *Masataka Higashiwaki*, Osaka Metropolitan University/NICT, Japan

We studied the effects of nitrogen (N) radical irradiation on device characteristics of vertical Ga₂O₃(010) fin field-effect transistors (FinFETs). A positive threshold voltage (V_{th}) shift for the nitridated FinFET from the V_{th} value for the non-nitridated one was observed. The in-plane uniformity of V_{th} was also improved for the nitridated FinFETs. Finally, a multi-FinFET with fin width of 300 nm showed superior device characteristics such as a V_{th} of +1.0 V, a specific on-resistance (R_{on}) of 9.5 m Ω cm², a breakdown voltage (V_{br}) of 1,213 V, and a power figure of merit (V_{br}^2/R_{on}) of 0.15 GWcm⁻². These results indicate that N radical irradiation can be a useful technique to fabricate normally-off Ga₂O₃ FinFETs with an excellent in-plane uniformity of device performance.

3:25pm IWGO-WeA-18 Enhancement-Mode Ga₂O₃ CAVETs with Improved Breakdown Voltage by Hot Implantation, **Jun Morihara**, Osaka Metropolitan University, Japan; *Daisuke Matsuo, Shun Konno, Kosuke Usui, Shinya Takemura*, Nissin Ion Equipment Co., Ltd., Japan; *Zhenwei Wang*, National Institute of Information and Communications Technology, Japan; *Romualdo Ferreyra*, Osaka Metropolitan University, Japan; *Kohei Tanaka*, Nissin Ion Equipment Co., Ltd., Japan; *Masataka Higashiwaki*, Osaka Metropolitan University, Japan

Normally-off operation is highly demanded for FETs to ensure fail-safe capability in high-voltage and high-power applications. Enhancement-mode (E-mode) Ga₂O₃ current aperture vertical FETs (CAVETs) fabricated using room-temperature Si- and nitrogen (N)-ion implantations have been demonstrated [1]. Overall on-state device characteristics of the CAVETs were decent; however, the off-state breakdown voltage (V_{br}) was as low as 263 V [1], which could be attributed to the insufficient recovery of crystal damage caused by the implantations. In this work, we employed hot ion implantation to minimize the crystal damage and enhance V_{br} .

We used *n*-Ga₂O₃ (001) epitaxial substrates having an *n*-Ga₂O₃ drift layer grown by halide vapor phase epitaxy. The CAVET fabrication process started with N hot implantation. N ions with a dose of 1×10^{14} cm⁻² were implanted into the *n*-Ga₂O₃ drift layer at 450°C, followed by activation annealing at 1000°C for 20 min in N₂ atmosphere. Subsequently, multiple Si implantations were performed at 300°C to form an *n*-channel layer, *n*⁺-access regions, and *n*⁺⁺-drain and source ohmic regions. The activation annealing of the Si implants was carried out at 800°C for 30 min. A 50-nm-thick Al₂O₃ gate dielectric was formed by atomic layer deposition on the channel layer. Source and drain ohmic electrodes, and gate electrodes were fabricated with Ti/Au and Ti/Pt/Au metal stacks, respectively. The aperture size and the Si-implanted channel area were 20 μ m and 210 $\times$ 25 μ m², respectively.

Drain current–drain voltage (I_d – V_d) characteristics showed that at a gate voltage (V_g) of +6 V, the CAVET exhibited near-linear I_d turn-on behavior in the low V_d range and quasi-saturation at $V_d \sim 20$ V, and reached the maximum I_d of 0.123 kA/cm² at $V_d = 40$ V. The I_d – V_g characteristics at $V_d = 20$ V provided a high I_d on/off ratio of 1×10^{11} , which can be attributed to superior current-blocking capability of the N-implanted region formed by hot implantation. The threshold V_g extracted from linear extrapolation of the I_d – V_g curve was +3.8 V, ensuring the E-mode normally-off operation. The off-state I_d leakage at $V_g = 0$ V monotonically increased with increasing V_d and saturated at $10^{-3} - 10^{-2}$ A/cm² for $V_d > 100$ V. Then, destructive breakdown occurred near the gate electrode edge at $V_d = 756$ V. All on- and off-state device characteristics of the CAVET in this work were superior to those of the previous one [1]. Among the improvements, the most significant was the threefold increase in V_{br} . These results indicate that the hot implantation process is effective in improving endurance of Ga₂O₃ CAVETs.

[1] M. H. Wong *et al.*, IEEE Electron Device Lett. **41**, 296 (2020).

3:40pm IWGO-WeA-21 Enhancement-Mode Vertical β -Ga₂O₃ U-Trench MOSFET with N-doped CBL and MOCVD regrown n⁺ Contact Layers, **Walid Amir**, Jiawei Liu, Surajit Chakraborty, University at Buffalo-SUNY; *Dongsu Yu, Md. Mosarof Hossain Sarkar, Hingping Zhao*, Ohio State University; *Uttam Singiseti*, University at Buffalo-SUNY

Due to its large bandgap (~ 4.8 eV) and strong critical electric field (~ 8 MV/cm), β -Ga₂O₃ has drawn a lot of attention as an ultra-wide-bandgap (UWBG) semiconductor for high-power applications. However, because traditional n⁺ contact methods rely on ion implantation followed by high-temperature activation annealing, which increases process complexity and may degrade material quality, the realization of cost effective and low-resistance ohmic connections is still difficult. In this work, we reduce thermal budget while preserving electrical performance by using a regrown n⁺ contact layer to create highly doped contact areas without post-implantation annealing.

The fabrication process started on commercially available Sn-doped (001) β -Ga₂O₃ substrates with a ~ 10 μ m HVPE-grown epitaxial drift layer. The CBL was formed by N-ion implantation at multiple energy levels followed by annealing in N₂ atmosphere to activate the nitrogen dopants. In contrast to the conventional approach of using Si-ion implantation for ohmic contact formation, which requires additional high-dose implantation steps, dedicated masking, and high-temperature activation annealing, this work introduces a regrown Si-doped n⁺ contact layer (~ 75 nm) with a high carrier concentration of $\sim 10^{18}$ cm⁻³ deposited directly by MOCVD epitaxial regrowth.

The ohmic contact quality was validated by transmission line model (TLM) measurements, yielding a transfer length $L_T = 0.13$ μ m, contact resistance $R_c = 0.38$ Ω -mm, sheet resistance $R_{sh} = 1389$ Ω /sq, and specific contact resistivity $\rho_c = 2.65 \times 10^{-7}$ Ω -cm². Transfer characteristics demonstrated normally-off operation with a clear threshold voltage of $V_{th} = 5$ V and an I_{on}/I_{off} ratio of 8.5×10^5 . From the output (I_d – V_{ds}) characteristics swept with $V_{gs} = 0$ to 20 V in 5 V steps, a peak current density exceeding 100 A/cm² was achieved, with an on-resistance $R_{on} = 94.6$ m Ω -cm².

Three-terminal off-state breakdown measurements were performed in Fluorinert (FC-40) liquid to suppress air arcing. At $V_{gs} = 0$ V, breakdown voltages of 920 V–980 V were recorded across three representative devices, demonstrating excellent device-to-device uniformity and robust blocking capability. The resulting Baliga figure of merit ($BFOM = V_{br}^2/R_{on}$) makes this work well competitive with state-of-the-art vertical β -Ga₂O₃ devices.

This work demonstrates a high-performance enhancement-mode vertical β -Ga₂O₃ trench-gate MOSFET with N-ion implanted CBL and a simplified ohmic contact scheme based on epitaxial n⁺ regrowth. The regrown n⁺ contact approach offers a practical, cost-effective, and thermally efficient alternative to ion-implanted contacts, without sacrificing electrical performance.

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