International Workshop on Gallium Oxide and Related Materials (IWGO-6)

Room ESJ 0202 - Session IWGO-TuA1

Heterogeneous Integration and other WBG and UWBG Oxides Beyond Ga_2O_3

Moderators: Nolan Hendricks, AFRL, **Man Hoi Wong**, The Hong Kong University of Science and Technology

2:00pm **IWGO-TuA1-1 Heterogeneous Gallium Oxide Integration and Vertical Device Technology**, ***Martin Kuball,*** University of Bristol, UK**INVITED**

Gallium Oxide (Ga_2O_3) devices offer potential to outcompete SiC technology though have still to prove their true potential including device reliability, We demonstrate pathways to enable heterogenous Ga_2O_3 growth on alternative substrates including Si, furthermore challenges and solutions to overcome in vertical device technology, including mitigation of trap states for improve device reliability.

2:25pm **IWGO-TuA1-6 >10 kV Vertical NiO_x/(011) β-Ga_2O_3 HJDs with PFOM >2.3 GW/cm2**, ***Yizheng Liu***, *Carl Peterson, Chinmoy Saha,* University of California at Santa Barbara*; Marko Tadjer,* Naval Research Laboratory*; Sriram Krishnamoorthy,* University of California at Santa Barbara

We report the fabrication and characterization of vertical NiO_x/β-Ga_2O_3 heterojunction diodes (HJDs) on 20-µm-thick/low-doped HVPE-grown (011) β-Ga_2O_3 with breakdown voltage beyond 10 kV, differential specific on-resistance ($R_{on,sp}$) at 43 mΩ·cm^2, and power figure of merit (PFOM) exceeding 2.3 GW/cm^2 on 60-µm dia. device. The parallel-plane breakdown electric field ($E_{Br,||}$) is extracted to be >5.3 MV/cm.

The NiO_x/(011) HVPE β-Ga_2O_3 HJD fabrication begins with a backside Ti/Au (50/350 nm) Ohmic metallization on n$^+$ β-Ga_2O_3 bulk substrate using e-beam evaporation followed by a 60-seconds rapid thermal annealing (RTA) at 470 °C in N_2. A ~28 nm of p$^-$ NiO_x is deposited on HVPE β-Ga_2O_3 drift region with a pre-patterned photoresist liftoff mask by optical lithography. Following the first layer NiO_x deposition, a self-aligned p^{++} NiO_x (~20 nm) contact layer is reactively sputtered. Then, a Ni/Au/Ni (50/100/150 nm) anode cap/metal hard mask stack is deposited via e-beam evaporation. The fabricated HJDs are later dry-etched ~2 µm into the β-Ga_2O_3 drift region below the heterojunction interface using BCl_3 inductively coupled plasma (ICP) at 200 W for edge termination. A ~1.5-µm-thick SiO_2 field plate oxide is sputtered conformally on the HJDs, then a Ni/Au (50/300 nm) field plate metal stack a with 20-µm edge extension (L_{FP}) is deposited on the oxide via e-beam evaporation to conclude the device fabrication.

The mesa-isolated/field plated (MI/FP) HJD with 60-µm dia. dimension shows rectifying behavior with an on/off ratio of 10^{10} and turns on at ~2 V forward bias with an on-state current density >60 A/cm^2. The capacitance-voltage (C-V) characteristics of the HJD reveals a built-in potential of 2.2 V and an average apparent charge density at 1.8×10^{15} cm^{-3}. The 60-µm dia. device exhibits a breakdown voltage > 10 kV with a corresponding $E_{Br,||}$ >5.3 MV/cm. MI/FP HJDs with 100-µm dia. also exhibits breakdown voltages at 6.5-7.3 kV. The $R_{on,sp}$ of the 60-µm dia. device is at 43 mΩ·cm^2, giving rise to a PFOM > 2.3 GW/cm^2, which approaches the material limit of 4H-SiC. The HJDs across various diode dimensions (60-µm dia. to 1-mm dia.) show consistent $R_{on,sp}$ values which indicates that there is no current spreading and the extracted $R_{on,sp}$ is accurate. The pulsed current-voltage (I-V) measurements with <1% duty cycle show that the 1-mm dia. HJD accomplishes >1.5 A absolute current value at 9 V on thick and low-doped HVPE-grown β-Ga_2O_3, which is comparable to the I-V characteristics of co-fabricated Schottky barrier diode (SBD) counterpart, indicating that the vertical MI/FP HJD is able to fully exploit the on-state potential of the epitaxial drift region.

2:40pm **IWGO-TuA1-9 Semiconductor Properties of Epitaxial NiGa2O4 Spinel That Forms at Ga_2O_3/NiO Interfaces**, *Kingsley Egbo, Anna Sacchi, M. Brooks Tellekamp,* ***Andriy Zakutayev,*** National Laboratory of the Rockies

β-Ga_2O_3 is one of the most promising ultra-wide band gap semiconductor materials due to its combination of intrinsic semiconductor properties and manufacturing scalability. Considering the difficulties associated with p-type doping of *β*-Ga_2O_3, alternative strategies involving the heteroepitaxial growth of p-type oxide layers have been explored as potential substitutes. For example, the use of p-NiO contacts to *β*-Ga_2O_3 has led to a demonstration of vertical power diodes with breakdown voltages over 10 kV. Our recent work has shown that the NiO/Ga_2O_3 may become unstable above 400 °C temperature, leading to uncontrolled formation of $NiGa_2O_4$ at the interface. Such high temperatures may be present due to intentional heating for NiO growth or unintentional hot spots during high-power operation, exacerbated by low thermal conductivity. However, the $NiGa_2O_4$ structure and properties remains relatively unknown due to the thinness of this naturally formed interphase.

This presentation will report on the intentional epitaxial growth and semiconductor properties of $NiGa_2O_4$ spinel layers that naturally form at Ga_2O_3/NiO interfaces used in electronic devices. Cubic spinel $NiGa_2O_4$ films of 10-50 nm thicknesses and low surface roughness (~ 2 nm) were grown using pulsed laser deposition at the *α*-Al_2O_3 and *β*-Ga_2O_3 substrate temperatures in the 300-900 °C. The optical absorption onset (3.6-3.9 eV) and thermal conductivity (4-9 W m^{-1} K^{-1}) vary systematically with substrate temperature due to varying Ni and Ga cation ordering on the spinel lattice. The valence band offset between $NiGa_2O_4$ and *β*-Ga_2O_3 is determined to be 1.8 eV. The $NiGa_2O_4$-based p-n heterojunction devices on Ga_2O_3 (001) substrates with 10^8 rectification ratio and 1.4 V turn-on voltage maintaining this diode behavior up to 600 °C operating temperature. These results highlight the potential of $NiGa_2O_4$ as a *p*-type interlayer to increase the performance and reliability of Ga_2O_3-based devices in high-power and high-temperature applications.

2:55pm **IWGO-TuA1-12 Breaking the 6 eV Barrier: Colossal Bandgap Electronics with Si Doped α-$(Al_xGa_{1-x})_2O_3$ by S-MBE**, ***Debaditya Bhattacharya,*** *Jacob Steele, Kazuki Nomoto, Naomi Pieczulewski,* Cornell University*; Preston Sorensen,* University of Nebraska - Lincoln*; Madhav Ramesh,* Cornell University*; Indika Senevirathna,,* Clark Atlanta University*; Mathias Schubert,* University of Nebraska - Lincoln*; David Muller, Huili Grace Xing, Darrell Schlom, Debdeep Jena,* Cornell University

Establishing a new material as a viable semiconductor platform can be done by meeting three fundamental criteria: the demonstration of controllable doping with mobile carriers, a measurable bandgap, and the successful fabrication of rectifying junctions or observation of transistor action. In this work, we demonstrate that Si-doped α-$(Al_xGa_{1-x})_2O_3$ grown by suboxide molecular-beam epitaxy on sapphire fulfills these three criteria [1-3]. Hall effect measurements verify semiconductor behavior through controllable n-type conduction. Vacuum UV ellipsometry confirms a channel bandgap of 6.71

Leveraging this platform, we realize the first CBG “AlphaDiodes” and “AlphaFETs.” The diodes exhibit an on-off ratio > 10^7 and a lateral breakdown field of ~12 MV/cm - among the highest values recorded for any semiconductor. The Pd-gated AlphaFETs demonstrate enhancement-mode (normally-off) operation with a threshold voltage of ~1 V, proving that the channel potential can be effectively modulated via electrostatic gating despite the extreme bandgap. While current density is currently limited by contact and access resistance at the regrown interfaces, the combined evidence of Hall transport, optical bandgap, and transistor action establishes α-$(Al_xGa_{1-x})_2O_3$ as a practical platform for high-voltage, high-efficiency electronics.

Crucially, this platform utilizes *m*-plane sapphire substrates. Sapphire offers a unique trifecta of benefits: it is an abundant, low-cost material produced at a massive industrial scale (with crystals reaching diameters up to 640 mm) [4], and its high structural quality allows for the growth of high-purity epitaxial layers. By achieving these device milestones on a native, readily available substrate, we break the historical bottleneck of small-scale, high-cost synthesis that has previously hindered ultra-wide bandgap materials like diamond and c-BN, providing a clear path for the scalable adoption of colossal bandgap semiconductors.

[1] Steele, J., et al. (2025).*APL Materials*, 13, 101117

[2] Steele, J., et al. (2024). *APL Materials*, 12, 041113

[3] Jinno, R., et al. (2021). *Science Advances*, 7, eabd5891

[4] Kang Sen, et al. (J. Synth. Cryst.), **50**, 1397–1401 (2021)

3:10pm **IWGO-TuA1-15 Thin-Film β-Ga2O3 Composite Substrates for Thermal Management Solutions**, ***Michael Liao,*** APEX Microdevices*; Mark Goorsky,* University of California Los Angeles*; Piyush Shah,* APEX Microdevices

We demonstrate successful fabrication of single-crystalline β-Ga_2O_3 composite substrates on either 4H-SiC or diamond for thermal management of high-power electronic devices. Direct wafer bonding, without the use of bonding interlayers, at room temperature with ~kPa of applied pressure is employed to heterogeneously integrate β-Ga_2O_3. Prior to bonding, β-Ga_2O_3 substrates are implanted with light-atoms to induce exfoliation and transfer of single-crystalline β-Ga_2O_3 films to a handle

substrate such as 4H-SiC and diamond upon annealing. Leveraging our previous efforts on β-Ga_2O_3 exfoliation [1-3] and CMP [4], we continue to improve and expand key processing steps towards pristine thin-film β-Ga_2O_3 composite substrates for different β-Ga_2O_3 orientations including, but not limited to, (001), (010), and (100). We also develop post-bond wafer-stock removal (lapping and polishing) processes for achieving β-Ga_2O_3 composite substrates that require thicker β-Ga_2O_3 films that currently may not be commercially feasible via ion implantation (i.e., > 1 MeV). Thermal transport measurements comparing bulk β-Ga_2O_3 vs composite substrates subjected to the same heating conditions show a ~5× lower temperature rise and an effective thermal conductivity ~5 to ~10 times higher than bulk β-Ga_2O_3 depending on the film thickness. Thermal boundary conductance values for the β-Ga_2O_3|4H-SiC and β-Ga_2O_3|diamond interfaces are ~120 MW/(m^2K) and ~75 MW/(m^2K), respectively, which are on the same order achieved via β-Ga_2O_3 heteroepitaxy reported in the current literature. Unlike heteroepitaxy, which limits the β-Ga_2O_3 orientation typically to twinned ($\underline{2}$01) or polycrystalline depending on the substrate, wafer bonding bypasses limitations associated with heteroepitaxy to achieve structures with control over material combination and crystal orientation without sacrificing crystalline quality. To test robustness, thermal cycling of our β-Ga_2O_3composite substrates from room temperature up to 1000 °C show no degradation in the thermal transport across the interface. Subsequent homoepitaxial growth of device layers on these composite substrates will be presented.

The authors acknowledge the support from Air Force SBIR Phase II program. TPOC Dr. Thaddeus Asel.

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[2] M. E. Liao, et al., J. Vac. Sci. Technol. A, 41, 063203 (2023).

[3] M. E. Liao, et al., ECS Trans., 112(3), 269 (2023).

[4] M.E. Liao, et al., J. Vac. Sci. Technol. A, 41, 013205 (2023).

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