International Workshop on Gallium Oxide and Related Materials (IWGO-6)

Room ESJ 0202 - Session IWGO-FrM1

Plenary Session III

Moderators: Shizuo Fujita, Kyoto University, **Hongping Zhao**, The Ohio State University

7:15am **IWGO-FrM1-1 Breakfast**

8:00am **IWGO-FrM1-10 PLENARY: Scaling Ga_2O_3 Power Electronics: From 10 kV Devices to Megawatt Modules**, ***Yuhao Zhang,*** The University of Hong Kong **INVITED**

Benefiting from advances in large-diameter Ga_2O_3 wafers and processing technologies, Ga_2O_3 power device technology has made rapid progress in recent years. Reports of large-area, ampere-class Ga_2O_3 power devices have emerged worldwide, extending beyond fundamental research demonstrations to device packaging, circuit-level testing, and ruggedness evaluations. These milestones have established Ga_2O_3 as the only ultra-wide-bandgap (UWBG) semiconductor that has reached such critical steps toward practical commercialization and application.

This talk will introduce our recent progress on exploring Ga_2O_3 devices towards high-voltage, high-temperature, and high-power applications, addressing their critical barriers towards applications, and highlighting their potential to expand the frontier of power electronics.

Multidimensional device architectures—such as superjunction, FinFET, and multi-channel—can break the performance limit of 1D power devices and enable device performance improvements through geometrical scaling. To address the limitations in p-type doping in Ga_2O_3, we developed heterogeneous superjunctions based on charge-balanced NiO/Ga_2O_3 architectures. After the first demonstration of 2 kV Ga_2O_3 vertical superjunction devices [IEDM 23], we have demonstrated lateral NiO/Ga_2O_3 architectures superjunction diodes and transistors achieving breakdown voltages exceeding 10 kV and stable operation up to 250 °C [EDL 23, IEDM 24].

In parallel, scaling up current and power require advanced thermal management, particularly given the low thermal conductivity of Ga_2O_3. We explored the path of addressing the thermal challenge of Ga_2O_3 through packaging. We employed the junction-side cooling package to directly extract heat from the active junction and demonstrate a thermal resistance comparable to commercial SiC devices [T-PEL 21, EDL 22]. We then developed novel device-package interface designs for electrical-thermo-mechanical co-optimization, demonstrating the first ultra-wide bandgap power module capable of 1000 V, 200 A switching [IEDM 25]. Most recently, we upscale the power capacity of this module to megawatt and demonstrate its advantageous performance in pulsed power electronics applications [Nat. Commun. 26].

Reliability and robustness are also critical to power device applications. Despite the lack of effective p-type doping, we demonstrate the avalanche and surge robustness in NiO/Ga_2O_3 heterojunctions [Nat. Commun. 24], as well as good bipolar stability in this heterojunction [APL 25]. Overall, coordinated progress in device, packaging, and reliability is paving the way for deployment of Ga_2O_3 in next-generation power electronics.

8:45am **IWGO-FrM1-19 Formation of High-Quality SiO_2/β-Ga_2O_3 MOS Structures: Design and Optimization of Post-Annealing Processes**, ***Heiji Watanabe,*** *Kensei Maeda, Masahiro Hara, Takuma Kobayashi,* The University of Osaka, Japan **INVITED**

The metal–oxide–semiconductor (MOS) structure is a fundamental component in electronic devices. Among various insulators, SiO_2 is regarded as the most suitable material for Ga_2O_3–based electronics owing to its sufficiently wide bandgap, excellent insulating properties, and high thermal stability. For MOSFET operation, electrical defects at the insulator/semiconductor interface not only act as scattering centers in the MOS channel but also play a critical role in determining reliability factors such as threshold–voltage stability. Therefore, improving the MOS interface quality remains an important research challenge. However, only a limited number of studies have reported on SiO_2/Ga_2O_3 MOS structures [1], and research and development in this area is still in its early stages.

The fabrication of Ga_2O_3–based MOS devices inevitably involves the deposition of insulating films, for which post–deposition annealing (PDA) in an oxygen atmosphere is widely employed to improve film quality. In our study, SiO_2 films were directly deposited on wet–cleaned β–Ga_2O_3(001) substrates by plasma–enhanced chemical vapor deposition. We first investigated the impact of PDA on the electrical properties of SiO_2/β–Ga_2O_3 MOS capacitors [2]. Although high–temperature PDA in O_2 ambient effectively reduced electrical defects at the interface, it also caused a decrease in the net donor density in Ga_2O_3, suggesting the formation of deep acceptor–type defects, likely associated with oxygen interstitials or gallium vacancies. However, subsequent annealing in N_2 ambient restored the donor density to its initial value. As a result, the combined O_2 and N_2 annealing process yielded a low interface–state density (D_{it}) of approximately 10^{11} $cm^{-2}eV^{-1}$ near the conduction–band edge of Ga_2O_3. We also confirmed enhanced immunity to gate–bias stress, indicating improved long–term MOSFET reliability. Furthermore, we demonstrated the significant benefits of post–metallization forming–gas annealing (FG–PMA) for SiO_2/β–Ga_2O_3 MOS structures [3]. FG–PMA at relatively low temperatures below 400 °C effectively reduced both D_{it} and near–interface traps, leading to further improvements in device performance and long–term reliability. When FG–PMA was performed following the combined O_2 and N_2 annealing, an extremely low D_{it} in the low–10^{10} $cm^{-2}eV^{-1}$ range was achieved through hydrogen passivation of electrical defects in the SiO_2/β–Ga_2O_3 MOS system.

This work was partly based on results obtained from a project, JPNP22007, commissioned by NEDO.

[1]K. Kita *et al.*, ECS Trans. **92**, 59 (2019).

[2] T. Kobayashi *et al.*, Appl. Phys. Lett. **126**, 012108 (2025).

[3] K. Maeda *et al.*, Appl. Phys. Lett. **127**, 112107 (2025).

9:10am **IWGO-FrM1-24 Quaternary (AlxScyGa1−x−y)2O3 for Lattice-Matched β-Ga2O3 Heterostructures**, ***Kazuki Koreishi,*** Institute of Science Tokyo, Japan*; Kodai Niitsu,* National Institute for Materials Science, Japan*; Takuto Soma,* Tohoku University, Japan*; Kohei Yoshimatsu, Akira Ohtomo,* Institute of Science Tokyo, Japan

Bandgap engineering of β-Ga_2O_3 has been widely investigated for enhancing Baliga's figure of merit of the materials and for developing heterojunction-based devices. These studies employed the heteroepitaxy of a ternary $(Al_xGa_{1-x})_2O_3$ (AGO) alloy; however, a phase-pure and high-quality AGO epitaxial layer is practically limited to an Al content of approximately 20% and a certain layer thickness due to the lattice mismatch. In contrast, a quaternary (AlxScyGa1−x−y)2O3 (ASGO) is expected to exhibit a wider tunability of the bandgap energy (E_g) and layer thickness owing to its lattice matching to β-Ga_2O_3. Here, we have investigated the crystal structures and E_g of ASGO powders and thin films for future heterojunction-based power-device applications.

The four lattice parameters of the ASGO powder samples are identical to those of β-Ga2O3 when *x*/*y* is between 1.5 and 3.2. We thus prepared several ASGO films with the lattice-matched *x*/*y* range on β-Ga_2O_3 (100) by using pulsed-laser deposition. The lattice-matched ASGO (100) epilayer exhibited superior crystallinity as confirmed by a sharp reflection from the thin film in x-ray diffraction reciprocal space maps. The estimated E_g of the ASGO (100) films determined by electron energy loss spectroscopy varied from 4.5 to 5.8 eV while maintaining the lattice matching to β-Ga_2O_3.

9:25am **IWGO-FrM1-27 Characterization and Light Emission of CBLs with Varying Nitrogen Implantation Doses for β-Ga_2O_3 Devices**, ***Kohei Ebihara,*** *Tetsuro Hayashida, Munetaka Noguchi, Rina Tanaka, Ryuji Sakai, Hiroshi Watanabe, Masaki Taya, Tatsuro Watahiki,* Mitsubishi Electric Corporation, Japan

β-Ga_2O_3 has an ultrawide bandgap of 4.7 eV and superior material properties that make it a promising candidate for next-generation power devices. However, realization of effective p-type doping in β-Ga_2O_3 remains a significant challenge, limiting the performance of devices. To address this issue, current-blocking layers (CBLs) with deep levels introduced by nitrogen (N) ion implantation have been proposed as an alternative to p-type wells. In this study, CBL test element groups (CBL-TEGs) with varying N implantation doses were fabricated to evaluate CBL performance and reduce leakage current. Light emission analyses were performed to identify the leakage locations and elucidate the leakage mechanism.

CBL-TEGs have an epitaxial layer grown on a β-Ga_2O_3 (001) substrate, with a carrier concentration of 1.0×10^{16} cm^{-3} and a thickness of 10 µm. N ion implantation was performed to create a box profile with a depth of 0.8 µm. Total N doses were 4.0×10^{13}, 4.0×10^{14}, and 4.0×10^{15} cm^{-2}. An n^+ layer

with a depth of 0.2 μm was formed by silicon (Si) ion implantation. Following N and Si implantations, annealing was performed at 900 °C for 30 min. and 1 min., respectively. The top and bottom electrodes were formed by depositing Ti/Au with thicknesses of 20/230 nm. Finally, the top electrode was patterned, and the samples were annealed at 470 °C for 1 min.

The reverse-bias characteristics of the CBL-TEGs with various N doses were measured. Increasing the N dose effectively reduces the leakage current. Specifically, for the sample with a dose of 4.0×10^{15} cm^{-2}, the leakage current remained below 2×10^{-5} A/cm^2, a substantial improvement over previously reported values. After that, plan-view images of light emission and the emission spectrum under leakage condition were obtained. Clear emission is observed from the n^+ region surrounding the top electrode for the 4.0×10^{13} cm^{-2} sample, indicating that leakage current was distributed throughout the CBL under the entire n^+ region. An emission peak near 700 nm (1.77 eV) suggests electron transitions involving the deep level. For the 4.0×10^{14} cm^{-2} sample, emission from the n^+ region around the electrode was observed, as with the case for the 4.0×10^{13} cm^{-2} sample. In contrast, for the 4.0×10^{15} cm^{-2} sample, emission was confined to the edge of the n^+ region. These observations indicate that a N dose of 4.0×10^{15} cm^{-2} effectively suppresses leakage through the CBL under the n^+ region.

Acknowledgement: This study is based on results obtained from a project, JPNP22007, commissioned by the New Energy and Industrial Technology Development Organization (NEDO).

9:40am **IWGO-FrM1-30 Development of Surface Preparation Methods for Insulating and Conductive, Miscut (100) β-Ga_2O_3 Substrates**, ***Robert Lavelle***, *Luke Lyle, Benjamin Dutton, Connor Beakes, Eric Welp, Scott Pistner, Andrew Balog,* Penn State University*; Drew Haven, David Joyce,* Luxium Solutions*; Nasim Alem, Joan Redwing, David Snyder,* Penn State University

Encouraging epitaxial growth results on miscut (100) β-Ga_2O_3 substrates have motivated evaluation of this orientation for device applications. In addition to CMP, final substrate preparation is critical for facilitating high-quality epitaxial growth, especially for vicinal surfaces. Previous studies on insulating, Mg-doped substrates used phosphoric acid (H_3PO_4) etching and O_2 annealing steps prior to epitaxial growth. However, implementing this process resulted in significant surface roughening of Fe-doped substrates in this work. There is further motivation to utilize conductive substrates for higher power devices. These substrates also require alternative surface preparation steps as annealing in O_2 can result in passivation of the surface with Ga vacancies and a corresponding decrease in conductivity.

This study establishes surface preparation methods for both insulating, Fe-doped and conductive, Sn-doped miscut (100) β-Ga_2O_3 substrates. For both substrate types, an atomically smooth surface (Sq/rms <0.2 nm) with a uniform step/terrace structure was achieved by CMP followed by annealing at 850-900°C with a dwell time selected based on the miscut angle. For the Fe-doped substrates, reducing the total pressure was observed to be important for mitigating surface contamination with the optional inclusion of a hydrofluoric acid (HF) etching step (Fig. 1a). For the Sn-doped substrates, an epi-ready surface was also achieved by annealing in an inert, Ar atmosphere (Fig. 1b). Surface conductivity was maintained using a low O_2 partial pressure during annealing. However, Sn diffusion was observed, even at a relatively low temperature range, further emphasizing the importance of selecting appropriate surface preparation conditions for the miscut substrates. Overall, this study suggests that the surface ordering mechanism for miscut (100) β-Ga_2O_3 substrates is influenced by the Ga vacancy concentration and formation of defect complexes and/or diffusion via these sites. By controlling the variables that affect the formation/compensation of these vacancies, substrates can be prepared with vicinal surfaces for epitaxial growth.

9:55am **IWGO-FrM1-33 Analysis of Packaged Ga_2O_3 Schottky Barrier Diodes (SBDs) for AC Rectification at Industrial Voltages**, ***Jeremiah Williams***, KBR Inc.*; Nolan Hendricks, Joshua Piel,* AFRL*; Zachary Weber,* Ohio State University*; Aaron Adams, Weisong Wang,* KBR Inc.*; Kyle Liddy, Daniel Dryden,* AFRL*; Takekazu Masui, Higuchi Mitsuhito,* NCT, Japan*; Ahmad Islam, Andrew Green,* AFRL

This work analyzes Ga_2O_3 Schottky Barrier Diodes (SBDs) as half-wave AC rectifiers for a 473 V_{RMS} (669 V_{peak}) sine wave (Fig. 1). Fundamentally, transmitting power through higher voltage allows for lower currents, which improves system-level efficiency by reducing Joule heating and the requisite conductor weight [1]. We evaluate Ga_2O_3 diodes as AC rectifiers, a basic power-handling function, in voltage-dominated power transfer at voltages approaching the standard 480 V_{RMS} used for heavy industry in the USA.

The Ga_2O_3 devices in this analysis are packaged prototypes fabricated by Novel Crystal Technologies (NCT). They are compared to SiC devices fabricated by GeneSiC. Both devices use a TO-247 package. Table 1 contains measured diode characteristics. For half-wave rectifier testing, the diode is placed in series with an AC power supply and a variable resistor (the load). The power supply is set to source a 480 V_{RMS}, 1 kHz sine wave. An oscilloscope is used to measure V_{in}, V_{load}, and I_{load}. A sine or piece-wise function is fit to the measured data using SciPy for analysis. The efficiency of the diode is analyzed by comparing the on-state input power to the on-state output power minus the off-state output power. Thus, an ideal diode with no leakage or on resistance would be 100% efficient.

The efficiency of both the SiC and Ga_2O_3 diodes is ≈ 98%, dropping slightly as current increases (Fig. 2). This high efficiency is consistent with the I-V behavior. When delivering power with a higher voltage and lower current, the impact of the diodes' on resistance is reduced while that of the built-in voltage (V_{bi}) is emphasized. Some series resistance is introduced from the test setup, but it is the same for each device. Package temperature is measured with the load dissipating 88 W, corresponding to 538 mA peak current. The Ga_2O_3 diode measures slightly hotter throughout this test, ending at 26.7 ± 0.2 °C compared to the SiC diode at 26.0 ± 0.2 °C after three minutes. These results show that, despite lagging in on-resistance, the system-level performance of Ga_2O_3 SBDs is comparable to commercial SiC devices for voltage-dominated power transfer at 45-88 W.

10:25am **IWGO-FrM1-39 2.2 kV NiO Based JTE β-Ga_2O_3 Schottky Barrier Diode with Improved Reliability under High-Temperature Storage Stress**, ***Junpeng Wen***, *Xuanze Zhou, Guangwei Xu, Shibing Long,* University of Science and Technology of China

β-Ga_2O_3 power diodes havethe potential in applicationsat high-temperature and high-voltage environments. The NiO based junction termination extension (JTE) can prevent the diodes' premature breakdown, fully leveraging the high E_C of β-Ga_2O_3. However, the reliability of β-Ga_2O_3Schottky barrier diode (SBD) featuring JTE under high-temperature storage stress (HTSS) warrants attention. In this study, a HTSS test at 250 °C was conducted on JTE-SBD and the changes in device performance over the storage time were investigated. During the test, the turn-on voltage (V_{on}) of diodes increased from 0.90 V to 1.10 V, while the breakdown voltage (BV) showed a phenomenon of first increasing and then decreasing. The *C-V* measurements shows that the carrier concentration (N_A) of NiO initially decreases and subsequently increases, leading to the variations of the peak electric field. To enhance the device reliability, a 300 °C-10 mins oxygen annealing process has been proposed. By this approach, the V_{on} of JTE-SBD only increased 0.10 V during the test. Due to the lower and more stable N_A of NiO, the average BV of the annealed JTE-SBD maintained 2231 V even after 124 hours HTSS. Finally, XPS spectra illustrates the reasons for the changes of N_A of NiO. This study enhances the understanding of the reliability of β-Ga_2O_3 and NiO, providing effective strategy for improving the stability of NiO/β-Ga_2O_3 JTE-SBD.

10:40am **IWGO-FrM1-42 >1 GW/cm^2 β-Ga_2O_3 NiO_x Heterojunction Diodes on MOCVD-Grown (110) and (010) Epilayers**, ***Carl Peterson***, *Yizheng Liu, Chinmoy Nath Saha,* University of California Santa Barbara*; Jacob H. Leach,* Kyma Technologies Inc.*; James S. Speck, Sriram Krishnamoorthy,* University of California Santa Barbara

We report on the creation of >1 GW/cm^2 NiO_x field-plated heterojunction diodes (FP-HJDs) on MOCVD-grown (110) and (010) drift layers achieving breakdown voltages of up to 7.58 kV and parallel-plane critical electric fields ($E_{||}$) of up to 4.14 MV/cm. MOCVD epilayers were grown on conductive Sn-doped β-Ga_2O_3 (010) and (110) substrates using TMGa, O_2, Ar carrier gas, and SiH_4 as the silicon dopant source. Intentionally Si doped 40 μm and 6.2 μm epitaxial films were grown on the (110) and (010) substrates respectively. The 40 μm film was CMP polished for 1 hr. which smoothed the surface and reduced the epilayer thickness to ~25 μm. The sample surface exhibited global variation in height, but locally smooth surfaces for devices. The anode for the circular field-plated HJDs was created by depositing a stack of 27 nm p^- NiO_x, 20 nm p^+ NiO_x, and Ni/Au/Ni metal. Next, a 2 μm deep self-aligned etch was performed via a BCl_3 ICP process to isolate the p-n junction. Finally, a 1 μm thick SiO_2 FP dielectric, Ni/Au FP metal, and a Ti/Au backside Ohmic contact were deposited. High voltage C-V showed a flat N_D-N_A concentration of 2.5×10^{16} cm^{-3} and 5×10^{15} cm^{-3} for the (010) and (110) epilayers respectively. J-V measurements on the 6.2 μm (010) epi resulted in J = 700 A/cm^2 at 4 V, HJD ideality factors of 1.29, V_{bi} of 2 V, rectification ratio of 10^{11}, and a differential specific on resistance ($R_{On,sp}$) value of 2.36 mΩ.cm^2. Breakdown on the (010) epi was 1.64 kV, leading to a $E_{||}$of 4.02 MV/cm and a PFOM of 1.14 GW/cm^2. J-V on

the ~25 µm (110) epi resulted in J = 100 A/cm^2 at 5.6 V, HJD ideality factors of 1.08, V_{bi} of 1.8 V, rectification ratio of 10^{10}, and a $R_{On,sp}$ value of 32.2 mΩ.cm^2. Breakdown on the (110) epi was 7.58 kV, leading to a $E_{||}$of 4.14 MV/cm and a PFOM of 1.78 GW/cm^2. HJD results on the (010) and (110) epilayers are state-of-the-art, with $E_{||}$ and PFOM values rivalling those achieved on commercial HVPE (001) epilayers. Additionally, this is the first demonstration of devices on (110) epilayers, with the (110) results showing high promise for the material orientation.

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