## **Crystal Growth and Interface Engineering of Sn-related Group-IV Alloy Semiconductor for Device Applications**

O. Nakatsuka<sup>1,2</sup>, M. Kurosawa<sup>1</sup>, S. Shibayama<sup>1</sup>, and M. Sakashita<sup>1</sup> Grad. Sch. Eng., Nagoya Univ., Furo-cho, Chikusa, Nagoya 464-8603, Japan <sup>2</sup> IMaSS, Nagoya Univ., Furo-cho, Chikusa, Nagoya 464-8601, Japan

Sn-related group-IV alloy semiconductors, GeSn and GeSiSn have much attracted on those unique material properties; an indirect-direct transition, a high carrier mobility, a good responsivity for near- and mid-infrared lights, a low growth temperature, a low thermal conductivity, etc <sup>[1]</sup>. Also, the heterostructures of those alloy semiconductors realize rich energy band engineering for not only the band gap but also the band offsets like group-III-V compound semiconductors. These characters promise improved and/or superior electronic, optoelectronic, and thermoelectric device applications integrated on Si large scale integrated circuit platform.

We have developed the crystal growth technology of epitaxial and polycrystalline Sn-related group-IV alloy semiconductor thin films for device applications<sup>[1]</sup>. There are some difficulties of the crystal growth of GeSn thin films; the low thermal-equilibrium solid solubility of Sn in Ge as low as 1%, also we have to take care for dislocations and defects with the strain relaxation on Si substrate and the low growth temperature. We need to establish the engineering technology of crystal growth and heterostructure formation with GeSn and GeSiSn to control the electrical properties. Recently, we achieved the thin film growth of a GeSn epitaxial layer with an ultra-high-Sn content over 50%<sup>[2]</sup>. A key point for realizing such a high Sn content is the lattice-constant engineering of substrate for epitaxial growth. We used a large-lattice-constant substrate of GaSb whose lattice matches to that of Ge<sub>0.48</sub>Sn<sub>0.52</sub> to suppress the strain between epitaxial layer and substrate.

We also achieved the heteroepitaxial growth of GeSn/GeSiSn multi layers for providing a double barrier structure. Those realize the carrier confinement structures at the valence and conduction band edges. We demonstrated its effectiveness improving optoelectronic properties enhancing photon-electron response<sup>[3]</sup> and recently realizing the resonant tunneling diode operating at room temperature<sup>[4]</sup>.

The development of interface engineering technology on insulator/GeSn and metal/GeSn systems is also a key issue for high-performance devices. In our presentation, we will introduce our recent achievements in an Al<sub>2</sub>O<sub>3</sub>/GeO<sub>2</sub>/GeSn structure for surface passivation<sup>[5]</sup> and low-resistance NiGe(Sn)/Sb-doped Ge(Sn) contacts<sup>[6]</sup> for electronic and optoelectronic device applications.

This work was partly supported by JST ASPIRE (JPMJAP2413), JST CREST (No. JPMJCR21C2), and JST PRESTO (No. JPMJPR21B6).

[1] S. Zaima *et al.*, Sci. Technol. Adv. Mater. **16**, 043502 (2015). [2] S. Shibayama *et al.*, Appl. Phys. Express **17**, 115503 (2024). [3] M. Fukuda *et al.*, Semicond. Sci. Technol. **33**, 124018 (2018). [4] S. Torimoto *et al.* ACS Appl. Electron. Mater. **7**, 7688 (2025). [5] Y. Kato *et al.*, *in Ext. Abstra. of SSDM2024*, Himeji, Japan (2024). [6] J. Jeon *et al.*, Semicond. Sci. Technol. **33**, 124001 (2018).

<sup>&</sup>lt;sup>+</sup> Author for correspondence: nakatsuka@nagoya-u.jp